Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **A**
2. **B**
3. **C**
4. **D**
5. **E**
6. **F**
7. **GND**
8. **Y**
9. **N/C**
10. **N/C**
11. **G**
12. **H**
13. **N/C**
14. **VCC**

**DRAFT**

**.057”**

**.052”**

**2 1 14 13**

**12**

**11**

**10**

**6 7 8 9**

**3**

**4**

**5**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .052” X .057” DATE: 2/8/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .015” P/N: 54AS30**

**DG 10.1.2**

#### Rev B, 7/1